60. The memory device of claim [53] 73 wherein the ions are implanted into the substrate below [the dielectric-filled area] said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of [the dielectric-filled area] said first area filled with said first dielectric material.

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## REMARKS

Claim 58 stands rejected under 35 U.S.C. § 112, second paragraph, as being identical to claim 54. Claim 58 has been cancelled.

Claims 43, 44 and 53 have been cancelled and the subject matter thereof has been represented in new claims 68, 69, 70, 73 and 74. Claims 71, 72, 75 and 76 have been added.

Claims 45, 46, 49-52, 54, 55, 57, 59 and 60 have been amended.

Claims 43-46 and 49-52 stand rejected under 35 U.S.C. § 103 as unpatentable over Schuegraf et al. (U.S. Patent No. 5, 702, 976) in view of Jeng (U.S. Patent No. 5, 706, 164). The rejection is traversed with respect to the amended claims.

The claimed invention relates to a semiconductor substrate including an isolation trench. As new independent claim 68 recites, the isolation trench includes "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls." Independent claim 68 further recites "an ion implanted region" situated below the second

area with "substantially all ions from said ion implanted region being displaced away from said separated active regions."

Schuegraf et al. ("Schuegraf") relates to a trench isolation process for alleviating the void formation during dielectric refill. (Col. 2, lines 49-52). To achieve this, Schuegraf proposes a dielectric material with a lower dielectric constant than used in the prior art. (Col. 4, lines 39-40). Indeed, the trenches in Schuegraf are "refilled with a dielectric material" with low dielectric constant (Col. 3, lines 61-62). However, none of these trenches have a first and a second areas which are filled with corresponding dielectric materials, as new independent claim 68 of the present invention recites. Further, Schuegraf does not teach or disclose an ion implanted region directly below the second dielectric area.

To overcome the shortcoming of Schuegraf, the Examiner relies upon Jeng and asserts that "[I]mpurity dopants in a substrate are conventional, as applicant would agree and as shown by Jeng et al (sic) (column 3)." (Office Action at 2). Jeng teaches a method for increasing the surface area of a stacked capacitor by using, *inter alia*, an elevated trench isolation structure. (Col. 2, lines 19-24). Jeng does not disclose either a trench isolation structure with "a first area filled with a first dielectric material . . . and a second area filled with a second dielectric material" or ion implantation directly below the second area. Thus, there is no teaching or suggestion in either of these two references, either independently or combined, for the subject matter of claims 68-72, 45-46, and 49-52.

Claims 45, 46 and 49-60 stand rejected under 35 U.S.C. § 102 as being anticipated by either Jeng or Narita (U.S. Patent No. 5, 859, 451). This rejection is traversed with respect to the amended claims.

The claimed invention relates to a semiconductor structure including an isolation trench which is first partially filled with "a first dielectric material" and then filled with "a second dielectric material," as new independent claims 68 and 73, and new dependent claim 69 recite. As newly added claims 71-72 and 75-76 recite, the first and second dielectric materials can be the same or different. As independent claims 68 and 73 further recite, the trench structure also includes "an ion implanted region . . . below said second area" containing ions which "are displaced away from said separated active regions." New independent claim 73, as well as new dependent claim 70, further recite that "substantially all ions from said ion implanted region being displaced away from said separated active regions by a distance at least equal to a sidewall thickness of said first area."

Jeng does not disclose any of the limitations of the claimed invention. Jeng teaches only a method for increasing the surface area of a stacked capacitor by using an elevated trench isolation structure, (Col. 2, lines 19-24). Jeng does not disclose or even mention an isolation trench with two dielectric material areas or "an ion implanted region below" the second area, with all implanted ions being displaced away from said separated active regions. The only mention to ion implantation in Jeng is the doping of polysilicon via ion implantation, as a well-known method. (Col. 3, lines 25-30). Accordingly, the claimed invention is not anticipated by Jeng under § 102.

Similarly, Narita does not disclose "an ion implanted region below said second area," or first and second areas which are respectively filled with a first and second dielectric material, and with all implanted ions displaced away from the separated active regions, as new independent claims 68 and 73 recite. Narita is silent about the existence of an isolation trench in a semiconductor substrate, or about an ion implanted region situated directly below a second area filled with a dielectric material. Accordingly, the claimed invention is not anticipated by Narita under § 102.

Claims 43-44, 46-55 and 57-60 stand rejected under 35 U.S.C. § 102 as being anticipated by Kohara et al. (U.S. Patent No. 4, 799, 093). This rejection is also inapplicable to the amended claims.

New independent claims 68 and 73 recite "a first area filled with a first dielectric material forming at least sidewalls of said isolation trench" as well as "a second area filled with a second dielectric material situated within the sidewalls," as part of a field isolation region. As newly added claims 71-72 and 75-76 recite, the first and second dielectric materials can be the same or different. New independent claims 68 and 73 further recite "an ion implanted region" situated "below said second area" containing ions displaced away from the separated active regions. In addition, newly added claims 70 and 73 recite ions displaced away from the active regions "by a distance at least equal to a sidewall thickness of said first area."

Kohara et al. ("Kohara") discloses neither areas filled with dielectric materials nor an ion implanted region formed directly below them and as part of a field isolation

region. Kohara teaches a method for reducing the surface area of a memory cell by employing a superposed capacitor. (Col. 1, line 68; Col. 2, lines 1-3). Kohara is also silent about any ion displacement away from the active regions, as amended claims 68-73 of the claimed invention recite. Accordingly, none of the limitations of the present invention are described or mentioned in Kohara and, thus, the present invention is not anticipated.

Claims 43-45 and 49-52 stand rejected under 35 U.S.C. § 102 as being anticipated by Kooi et al. (U.S. Patent No. 3, 755, 001). The rejection is also inapplicable to the amended claims.

Kooi et al. ("Kooi") discloses a method of manufacturing semiconductor devices, during which a surface zone of a semiconductor body is doped with activators and an oxide pattern is provided on at least a part of the surface zone by local oxidation. (Col. 1, lines 4-9). Kooi does not disclose an isolation trench or "a second area filled with a second dielectric material" situated within sidewalls of "a first area filled with a first dielectric material," as new independent claims 68 and 73 recite. Further, Kooi does not disclose "an ion implanted region . . . below said second area," as new claims 68 and 73 also recite. Kooi is also silent about ion displacement, which is a limitation of new claims 70 and 73 of "substantially all ions from said ion implanted region being displaced away from said separated active regions" by a distance "at least equal to a sidewall thickness of said first area filled with said first dielectric material." Accordingly, the present invention is not anticipated by Kooi.

Claims 43-45 and 49-52 stand rejected under 35 U.S.C. § 102 as being anticipated by Doo (U.S. Patent No. 3, 386, 865). This rejection is also inapplicable to the amended claims.

Doo teaches a method of making planar semiconductor devices isolated by encapsulating oxide filled channels. (Col. 1, lines 2-4). As such, Doo discloses "isolating channels of the encapsulating $SiO_2$" below which "p+ regions of semiconductor material" are disposed, (Col. 3, lines 68-75), to provide heat dissipation. (Col. 5, line 21). Doo, however, does not disclose a first and second area filled with a first and second dielectric material, or "an ion implanted region" or ions which are displaced away from separated active regions," as new independent claims 68 and 71 recite. Thus, Doo does not anticipate the claimed invention.

Claims 43, 44 and 49-52 stand rejected under 35 U.S.C. § 102 as being anticipated by Mastroianni et al. (U.S. Patent No. 4, 443, 932). This rejection is also inapplicable to the amended claims.

Mastroianni et al. ("Mastroianni") discloses a self-aligned process for dielectrically isolated structures, which employs a master mask layer that can be selectively reopened so that different device regions are sequentially formed. (Col. 2, lines 44-63). In rejecting the claims, the Examiner points to Figure 3J of Mastroianni. In explaining the self-aligned process, Mastroianni refers to ion implantation regions, such as the P-base 126 with reference to Figure 3J. However, Mastroianni does not show or suggest "a second area filled with a second dielectric material" situated within the sidewalls of "a first area

filled with a first dielectric material," or "an ion implanted region . . . below said second area," as new claims 68 and 73 of the claimed invention recite. Mastroianni is also silent about ion displacement from the separated active regions "by a distance at least equal to a sidewall thickness of said first area" filled with said first dielectric material, as claims 68, 69 and 73 recite. Thus, again, the claimed invention is not anticipated by Mastroianni.

Claims 43-45 and 49-52 stand rejected under 35 U.S.C. § 102 as being anticipated by Custode et al. (U.S. Patent No. 4, 990, 983). The claims have been amended and the rejection is respectfully traversed.

Custode et al. ("Custode") discloses a field oxide region under which a heavily doped region is formed to increase threshold voltages. (Col. 1, lines 29-34). As such, a "heavily doped (degenerate) p+ region 13" is formed immediately beneath "thin oxide notched regions 11." (Col. 4, lines 19-23). Custode does not disclose "an ion implanted region . . . below said second area," or "substantially all ions" from the ion implanted region being "displaced away from said separated active regions," as new independent claims 68 and 73 recite. Further, while the claimed invention is directed to an ion implanted region as part of a field isolation region, the heavily doped (degenerate) p+ region 13 of Custode is not part of a field isolation region. Thus, again, the present invention is not anticipated by Custode.

Finally, claims 43, 44, 46 and 49-52 stand rejected under 35 U.S.C. § 102 as being anticipated by Joo et al. (U.S. Patent No. 5, 841, 163). This rejection is also inapplicable to the amended claims.

Joo et al. ("Joo") teaches a method for fabricating a memory cell by employing a first and second field insulation layers coupled with a first and second channel stop impurity layers. (Col. 3, lines 38-48). For example, Joo discloses that impurity ions are implanted below the second field oxide layer and are diffused by a thermal process to form a first channel stop impurity layer. (Col. 6, lines 1-3). However, Joo does not disclose first and second areas filled with first and second dielectric materials, or an ion implant region below the second area, or that substantially all ions in the implant region are displaced away from the separated active regions, as new independent claims 68 and 73 recite. Joo also fails to disclose or suggest the ion spacing limitations recited in new claims 70 and 73. Accordingly, the present invention is not anticipated by Joo.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

Attorney for Applicant